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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/746,823	12/22/2000	Erik Bengtsson	8194-453IP	8910

20792 7590 03/10/2004

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EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2631	7

DATE MAILED: 03/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/746,823	Applicant(s) BENGTSSON ET AL.	
	Examiner Khanh Tran	Art Unit 2631	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Amendment filed on 12/11/2003 has been entered. Claims 1-36 are pending in this Office action.

Response to Arguments

2. Applicant's arguments, see pages 2-6 of the Amendment, filed on 12/11/2003, with respect to the rejection(s)of claim(s) 1, 3-10, 12, 15-20, 22-28, 30, and 33-36 under 35 U.S.C 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Holden et al. U.S. Patent 6,411,655 B1, Lampe U.S. Patent 5,313,173.

Specification

3. The abstract of the disclosure is objected to because the abstract title *"I/Q Modulation Systems and Methods that Use Separate Phase and Amplitude Signal Paths and Perform Modulation within a Phase Locked-Loop"* should be deleted. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3-9, 20 and 22-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holden et al. U.S. Patent 6,411,655 B1.

Regarding claim 1, Holden et al. invention is directed to a modulation system and method that can efficiently modulate a signal onto a radio frequency carrier. In column 5 lines 41-65, Holden et al. discloses in figure 1 a modulation system including a digital signal processor (DSP) 10 supplying a sequence of phase values theta together with sequences of each of a number 'n' of *amplitude control bits* b1, b2 ... b(n). The phase sequence is applied to a phase modulator 11 along with a carrier frequency signal, to phase modulate the carrier frequency signal. Figure 4 illustrates the phase modulator 11 comprising an IQ modulator including a phase splitter 20 and a pair of modulators 21 and 22, which together generate a pair of in-phase, quadrature-phase signals. Holden et al. does not expressly disclose the in-phase, quadrature-phase signals and amplitude control bits from a baseband signal. However, one of ordinary skill in the art will appreciate that those signals are generated from a baseband signal according Holden et al. teachings.

The phase modulator 11 in figure 4 further shows a phase comparator 25, a loop filter 26, a voltage-controlled oscillator (VCO) 23, and a down-converter

24. Even though Holden et al. does not expressly teach a phase locked loop in the invention; however, one of ordinary skill in the art will appreciate that the IQ modulator, and the components 23 24 25 26 form a phase locked loop as claimed in the patent application. *Examiner's comment*: a similar PLL structure (e.g. see figure 3) having same components is disclosed in another US Patent 6,018,275.

As described in column 4 lines 31-43, Holden et al. invention utilizes multiple saturated power amplifiers 12 in figure 1 to approximate a linear power amplifier. Hence, it would have been obvious for one of ordinary skill in the art at the time the invention was made that the combination of saturated power amplifiers 12 forms linear power amplifier having a signal input connected to the phase modulator 11, a combining output connected to an antenna. Figure 4 shows the output of VCO 23 is connected to power amplifiers 12. Furthermore, since multiple saturated power amplifiers 12 in figure 1 utilized to approximate a linear power amplifier, one of ordinary skill in the art will appreciate that all amplitude control bits b1, b2, ..., b(n) form an equivalent amplitude control signal inputted to the amplitude control input of the equivalent linear power amplifier.

Regarding claim 3, referring back to figure 1, the DSP 10 converts a stream of complex numbers into polar form, including an amplitude-representative part and a phase-representative part. Those skilled in the art would appreciate that the in-phase

and quadrature-phase signals are normalized by the conversion process, and the modulated signal is a constant amplitude modulated signal.

Referring to figure 4, a constant frequency signal referred to as the Transmit Intermediate Frequency (TXIF) is supplied to an IQ modulator including a phase splitter 20 and a pair of modulators 21 and 22. The phase splitter 20 generates two TXIF signals 90 degrees apart in phase. Balanced modulator 21 applies the cosine of the phase value theta to the cosine modulator 21, and the sine of theta to the sine modulator.

Regarding claim 5, Holden et al. discloses in the abstract that a stream of complex numbers is converted into polar form, including an amplitude-representative part and a phase-representative part. Those skilled in the art will appreciate that the amplitude-representative part is a square root of a sum of the in-phase signal squared and the quadrature-phase signal squared.

Regarding claim 6, as recited in claim 1, Holden et al. utilizes multiple saturated power amplifiers 12 in figure 1 to approximate a linear power amplifier 12. Figure 4 also shows all amplitude control bits b1, b2, ..., b(n) controlling individual power amplifiers 12. Hence, the amplitude control bits b1, b2, ..., b(n) also form an equivalent amplitude control signal to the equivalent linear power amplifier. Holden et al. does not show a power control signal as claimed. However, as well known in the art of amplifiers, the

power control signal of an amplifier is just a gain control signal, which is used to adjust power gain in most amplifiers. Since amplitude control and gain control are related to each other, one of ordinary skill in the art will appreciate that the equivalent amplitude control input of the approximate linear power amplifier 12 would be responsive to the amplitude control signal and to the power control signal.

Regarding claim 7, Holden et al. invention utilizes multiple saturated power amplifiers 12 shown in figure 1 to approximate a linear power amplifier. The combined output is connected to an antenna as shown in figure 1. Holden et al., however, does not disclose employment an amplifier in conjunction with a power amplifier. Nevertheless, one of , one of ordinary skill in the art will appreciate that such implementation is well known in the art and is just a design choice.

Regarding claim 8, in addition to the rejection argument of claim 1, figure 1 shows an antenna responsive to the combining output 13 of power amplifiers 12. one of ordinary skill in the art will appreciate that the DSP 10 is responsive to a user interface that generates a baseband signal in response to a user input as claimed in the patent application.

Regarding claim 9, as recited in claim 1, , Holden et al. employs multiple saturated power amplifiers 12 shown in figure 1 to approximate a linear power amplifier.

Regarding claim 20, said claim has similar scope with claim 1, therefore, the rejection argument of claim 1 also applies here.

Regarding claim 22, said claim has similar scope with claim 3, therefore, the rejection argument of claim 3 also applies here. Furthermore, the amplitude-representative part is also a normalized amplitude signal.

Regarding claim 23, the rejection argument of claims 3-4 addresses all claimed limitations.

Regarding claim 24, said claim has similar scope with claim 5, therefore, the rejection argument of claim 5 also applies here.

Regarding claim 25, said claim has similar scope with claim 6, therefore, the rejection argument of claim 6 also applies here.

Regarding claim 26, referring to figure 1 again, the modulated signal is amplified by power amplifiers 12 and is transmitted through the antenna.

Regarding claim 27, said claim has similar scope with claim 8, therefore, the rejection argument of claim 8 also applies here.

5. Claims 2 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holden et al. U.S. Patent 6,411,655 B1 as applied to claim 1 above, and further in view of Lampe U.S. Patent 5,313,173.

Regarding claims 2 and 21, referring back to figure 4 of Holden et al. invention, the phase modulator 11 (equivalent to a PLL as discussed in claim 1 includes a voltage controlled oscillator input of VCO 23 through the loop filter 26. Holden et al. discloses a feedback loop having a mixer 24 responsive to a local oscillator F_{1o} in the phase modulator 11, but not configured in the same way as claimed in the patent application. Furthermore, Holden et al. invention does not teach the IQ modulator located in one of the claimed positions in the feedback loop.

Lampe discloses in another US patent a phase-locked loop (shown in figure 3) incorporating a quadrature modulator 340 for generating constant envelope phase or frequency modulation. According to Lampe teachings in the abstract, locating the quadrature modulator 340 in the feedback loop permits accurate constant envelope phase modulation of the loop reference oscillator. The PLL in figure 3 includes a frequency prescaler 305 for downconverting the frequency of the output from quadrature modulator 340. Those skilled in the art would appreciate that the frequency prescaler 305 is equivalent to a mixer responsive to a local oscillator. The quadrature modulated PLL differs from the phase modulator 11 as taught by Holden et al. is that the feedback loop is between the VCO output and the VCO input, and the quadrature modulator is in the feedback loop between the VCO output and the prescaler 305. Hence, it would have been obvious for one of ordinary skill in the art at the time the

invention was made that Holden et al. phase modulator could be modified to incorporate Lampe teachings since both Lampe quadrature modulated PLL and Holden et al. phase modulator would generate the same constant envelope phase or frequency modulation. Furthermore, as disclosed in the patent application on page 16 lines 31-34, the positions of the modulators as claimed would produce the same result as appreciated by one of ordinary skill in the art. Therefore, implementing the quadrature modulator in the feedback loop as taught by Lampe into Holden et al. phase modulator would not impact the operation of phase modulator.

6. Claims 10, 12, 16-19, 28, 30 and 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al. U.S. Patent 6,631,254 B1.

Regarding claims 10 and 28, Wilson et al. discloses in figure 1 one embodiment of the invention. In column 2 line 4 through column 3 line 38, I and Q-quadrature components of a baseband signal are applied to mixers 2a and 2b that mix them with components of a reference signal. The mixers 2a and 2b forms a quadrature modulator that modulates the I and Q-quadrature components of a baseband signal as claimed in the patent application.

A phase locked loop includes a phase detector 6, a VCO 8 having an output connected to a pre-driver 9. Wilson et al. does not expressly disclose a phase tracking subsystem and the quadrature modulator is included within the PLL. One of ordinary skill in the art will appreciate that the quadrature modulator could be considered to be part of the PLL. Furthermore, it would have been

obvious to one of ordinary skill in the art at the time the invention was made that the PLL as taught above is part of phase tracking subsystem since the PLL only tracks phase of the modulated signal. The PLL further is responsive to the quadrature modulator to produce a phase signal that is responsive to phase changes in the modulated signal. From figure 1, the phase signal is independent of amplitude changes of the modulated signal.

The modulated signal is amplitude limited by a limiter 5, and the amplitude signal is applied to one input of a differential amplifier 16. The signal picked-off from the directional coupler 13 is rectified and applied to the other input of the differential amplifier 16, which operates as an integrator and controls the gain of an RF power amplifier 11. Wilson et al. does not expressly disclose an amplitude tracking subsystem. However, one of ordinary skill in the art will appreciate that the path through the differential amplifier 16 and the feedback loop through the diode 15 forms an amplitude tracking portion. It should be clear from figure 1 that the amplitude tracking portion is responsive to the quadrature modulator to produce an amplitude signal that is responsive to amplitude changes in the modulated signal and that is independent of phase changes of the modulated signal.

A power amplifier 11 has an input responsive to the phase signal produced by the PLL, an output, and gain control input responsive to the amplitude signal.

Regarding claims 12 and 30, as recited in claim 10, the path through the differential amplifier 16 and the feedback loop through the diode 15 forms an amplitude tracking portion. The differential amplifier 16 automatically controls the gain of the PA 11 in response to the feedback RF output 12 and the input amplitude signal of the modulated signal.

Regarding claims 16 and 34, referring back to figure 1, a limiter 5 is employed between a quadrature modulator 2a 2b and the PLL.

Regarding claims 17 and 35, Wilson et al. invention does not show another power amplifier after the PA 11 and an antenna for transmission. However, such configuration is well known in the art of transmitters and the implementation is just a design choice.

Regarding claims 18 and 36, Wilson et al. does not show a transmit antenna in figure 1 at the RF output. However, the transmit antenna is inherently at the RF output. Furthermore, one of ordinary skill in the art will appreciate that I and Q components are inputted from a user through a user interface.

Regarding claim 19, referring back to figure 1, the apparatus further includes a power amplifier 11.

7. Claims 11 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al. U.S. Patent 6,631,254 B1 as applied to claim 10 and further in view of Lampe U.S. Patent 6,631,254 B1.

Regarding claims 11 and 29, referring back to figure 1 of Wilson et al. invention, the VCO 8 includes an input, a feedback loop between the RF output 12 through a mixer 18, a limiter 19 to the phase detector 6 (between VCO input and VCO output). The mixer 18 is responsive to a local oscillator (LO) input. Wilson et al. does not show the quadrature modulator is in the feed back loop between the locations as claimed. Lampe invention discloses a quadrature modulator inserted in the feedback loop of a PLL between a VCO output and a prescaler 305 as shown in figure 3. The prescaler 305 is for downconverting the frequency of the output from quadrature modulator 340. One of ordinary skill in the art will appreciate that the prescaler 305 includes a mixer and a local oscillator to perform a downconverting process. As disclosed in the patent application on page 16 lines 31-34, the positions of the modulators as claimed would produce the same result as appreciated by one of ordinary skill in the art. Therefore, it would have been obvious for one of ordinary skill in the art at the time the invention was made that the quadrature modulator in figure 1 of Wilson et al. invention could be implemented in the feedback loop as taught in Lampe invention since location of the quadrature modulator in the feedback loop would not have any operational impact on the apparatus in Wilson et al. invention.

8. Claims 13-15 and 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al. U.S. Patent 6,631,254 B1 as applied to claim 10 and further in view of Cordoba U.S. Patent 6,671,337 B1.

Regarding claims 13 and 31, Wilson et al. does not disclose the envelope detectors and comparator as claimed. Cordoba discloses in figure 1 a transmitter having very similar structure to the apparatus as disclosed in Wilson et al.. The transmitter as taught by Cordoba also utilizes separate paths for phase signal and amplitude signal. Cordoba further includes an envelope detector 22 responsive to the modulated signal M', an envelope detector 23 responsive to the PLL, and a comparator that is responsive to the envelope detectors 22 23. It would have been obvious for one of ordinary skill in the art at the time the invention was made that Wilson et al. apparatus can be modified to include envelope detectors and comparator as taught by Cordoba since Cordoba and Wilson et al. teachings are very similar.

Regarding claims 14 and 32, in addition similar rejection argument of claim 13, referring back to figure 1 of Cordoba invention, the signal input to envelope detector 23 is the feedback RF output through a coupler 19, attenuator 18, down-converter 17, and bandpass filter 21. Hence, the envelope detector 23 is also responsive to amplifier 11.

Regarding claims 15 and 33, as recited in claim 13, Wilson et al. does not disclose the envelope detector as claimed in the patent application. Cordoba discloses in figure 1 a transmitter having very similar structure to the apparatus as disclosed in

Wilson et al.. The transmitter as taught by Cordoba also utilizes separate paths for phase signal and amplitude signal. Cordoba further includes an envelope detector 22 responsive to the modulated signal M'. It would have been obvious for one of ordinary skill in the art at the time the invention was made that Wilson et al. apparatus can be modified to include envelope detector in the amplitude tracking portion as taught by Cordoba since Cordoba and Wilson et al. teachings are very similar.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Camp, Jr. et al. U.S. Patent 6,295,442 B1 discloses "Amplitude Modulation to Phase Modulation Cancellation Method in an RF Amplifier".

Yamamoto U.S. Patent 6,693,956 B1 discloses "Power Amplifier Having Negative Feedback Circuit for Transmitter".

Perrett et al. U.S. Patent 6,018,275 discloses "Phase Locked Loop with Down-conversion in Feedback Path ".

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 703-305-2384. The examiner can normally be reached on Tuesday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 703-306-3034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT